

## Claims

## 1. Circuit element comprising:

an input for receiving an external clock with a clock period duration;

an unit for providing the circuit element with information representing the clock period duration of the external clock; and

a unit for the temporal control of at least one signal in the circuit element on the basis of the information representing the clock period duration.

2. Circuit element according to claim 1, wherein the unit for the temporal control of the at least one signal on the basis of the information representing the clock period duration and on nominal time information ascertains a number of clock cycles or fractions of clock cycles of the external clock by which the input signal is to be delayed so as to control temporally the at least one signal.

3. Circuit element according to claim 1, wherein the unit for providing the information representing the clock period duration of the external clock includes a memory for storing data representing a clock period assigned to a clock frequency.

4. Circuit element according to claim 3, wherein the memory includes a register with a given number of data bits.

5. Circuit element according to claim 1, wherein the unit for the temporal control of the at least one signal has a phase-

locked loop for generating a multiple of the external clock frequency in the circuit element.

6. Circuit element according to claim 1, wherein the unit for the temporal control of the at least one signal has a delay-locked loop (DLL) for adjusting a delay on the basis of the clock frequency information provided.

7. Circuit element according to claim 1, wherein the circuit element is a memory element.

8. Circuit element according to claim 7, wherein the signal is a precharge signal and/or a refresh signal.